

ABSTRACT OF THE DISCLOSURE

The present invention provides a PLL frequency synthesizer suitable for improving even a spurious characteristic in a lock state while ensuring a high-speed lockup characteristic to thereby implement satisfactory communication quality. A switch circuit interposed between a low-pass filter (LPF) circuit and a voltage-controlled oscillator (VCO) is controlled based on a control signal (Scnt) to open/close control a feedback loop lying between the low-pass filter (LPF) circuit and the voltage-controlled oscillator (VCO). Namely, the switch circuit is opened according to a path-opening instruction of a feedback loop based on the control signal (Scnt) to open the feedback loop, thereby stopping the operation of the feedback loop. If this stop operation is controlled according to the control signal (Scnt) so as to be carried out during a period in which a pseudo correction pulse is outputted from a charge pump circuit for each phase comparison cycle of a phase comparator, then spurious generation incident to the pseudo correction pulse can be suppressed.

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